1 Metallization

1.1 Wiring

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The wiring of an integrated circuit can take up to 80 % of the chip's surface, that's why techniques habe been developed to stack the wiring on top of the wafer in multiple layers. The amount of wires with only one additional layer can be reduced about 30 %.

Between the wires, isolation layers (oxide) are deposited, the metal layers are connected through vertical interconnect accesses (via). In today's microchips there are seven or more layers integrated. Edges and steps have to be rounded since the conformity of the metallization layers is not very good. This leads to bottlenecks in which current densities are increased so that electromigration occurs. To remove edges and steps there are several possibilities for planarization.

1.1.2 BPSG reflow

The reflow technique uses doped glasses like phosphorus silicate glass (PSG) or boron phosphorus silicate glass (BPSG). In a high temperature process the glasses melt and result in an uniform surface. Due to high temperature this technique can't be used for planarization of a metallization layer.

1.1.3 Reflow back etching

On top of the wafer a layer of silicon dioxide is deposited which is at least as thick as the highest step on the wafer. Next the oxide is coated with a resist or polyimide layer which is thermal treated for stabilization. In dry etching, the resist/polyimide and the

silicon dioxide are removed with identical etch rates (selectivity of 1), thus resulting in a planished surface.

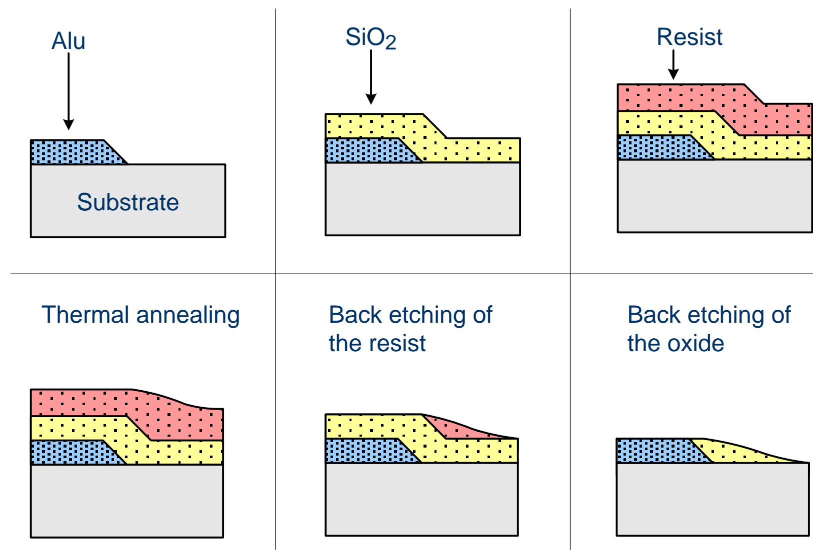


Fig. 1.1: Reflow back etching process

Besides the resist/polyimide, a so-called spin on glass (SOG) can be deposited on the wafer. Thus a planished layer can be produced which is stabilized during a post anneal step. An additional oxide layer is not necessary. However, all of these techniques can planish local steps only and are not sufficient for total leveling.

1.1.4 Chemical mechanical polishing

The chemical mechanical polishing/planarization (CMP) provides an uniform surface of the entire wafer. For this, an oxide is deposited on the wafer which is as thick as the highest step. The wafer is held upside down and pressed onto a polish plate. The wafer as well as the plate rotate in opposite directions and also move in horizontal directions. To support the process a slurry is used which contains abrasives and chemicals.

Even if this process seems to be very rough it allows a surface which has an irregularity of only a few nanometers and thus is the optimal process for planarization.

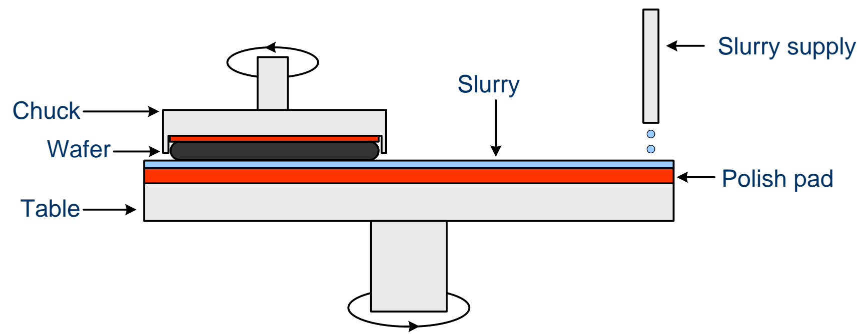
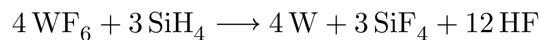


Fig. 1.2: Illustration of a polisher

1.1.5 Contacting

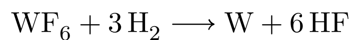
To contact the metallization layers, vias are etched into the isolation layers with high anisotropy. The vias have to be filled in this way, that an optimal contact is realized and the surface is not affected in a bad way.

For filling the vias, tungsten is the material of choice. With silane as additive a thin layer of tungsten is deposited as a seed layer in a CVD process with tungsten hexafluoride; byproducts as silicon tetrafluoride and hydrogen fluoride are exhausted:



$$4\,\mathrm{WF_6} + 3\,\mathrm{SiH_4} \longrightarrow 4\,\mathrm{W} + 3\,\mathrm{SiF_4} + 12\,\mathrm{HF}$$

With hydrogen as an additive to the tungsten hexafluoride the vias are filled thereafter:



$$\mathrm{WF_6} + 3\,\mathrm{H_2} \longrightarrow \mathrm{W} + 6\,\mathrm{HF}$$

On top if it the next metallization layer can be deposited, structured and planarized. If copper is used for wiring, tungsten will only be needed for the contact to the silicon substrate. The connection of the individual copper layers is done with copper itself.